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## INTELLECTUAL PROPERTY LAW

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\* NOT ADMITTED IN D.C.

Assistant Commissioner for Patents  
Washington, D.C. 20231

Attorney Docket: P56077

Sir:

Submitted herewith is the following patent application:

Inventor:      1) KWANG-JIN YANG  
                      2) JUN-HO KOH  
                      3) GIL-YONG PARK  
                      4) BONG-SIN KWARK

Title:      BIT-RATE INDEPENDENT OPTICAL RECEIVER AND  
                      METHOD THEREOF

Please find attached hereto an application for patent which includes: Specification and Abstract, Claims, original Declaration And Power of Attorney, Assignment, and a certified copy of the foreign priority document identified below:

Verified Showing of Small Entity Status: NO

Drawings: Formal drawings, 6 sheets, Figures 1 through 5

Claim of priority under 35 U.S.C. §119:      YES

\*\* The Republic Of Korea Application No. 32170/1999 filed on 5 August 1999.

FEE (see formula below): CHECKS ARE ENCLOSED (#36934 & #36935)

Basic Fee \$345/690 .....      \$690.00

### Additional Fees:

Total number of claims in excess of 20: 20 times \$9/18 .      \$360.00

Number of independent claims in excess of 3:    times \$39/78 .....

\$0.00

Multiple Dependent Claims \$130/260 .....

\$0.00

An Assignment is likewise enclosed: Recording Fee \$40 ..      \$40.00

Filing Non-English specification .....

\$0.00

**TOTAL FEES FOR THE ABOVE APPLICATION .....**      **\$1,090.00**

Assistant Commissioner for Patents  
20 July 2000  
Page Two

Docket No.: P56077

Inventor:    **1) KWANG-JIN YANG  
2) JUN-HO KOH  
3) GIL-YONG PARK  
4) BONG-SIN KWARK**

Title:        **BIT-RATE INDEPENDENT OPTICAL RECEIVER AND  
METHOD THEREOF**

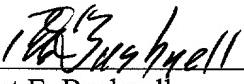
Assistant Commissioner is authorized to charge our Deposit Account No. 02-4943 for any additional charges necessary towards payment of the filing fee for the above-referenced application. Please notify the undersigned attorney of any transaction regarding our Deposit Account.

In view of the above, it is requested that this application be accorded a filing date pursuant to 37 CFR 1.53(b).

Please address all correspondence to:

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Respectfully submitted,

  
\_\_\_\_\_  
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07/20/00

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

# FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.

These are the fees effective October 1, 1997.

Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

See 37 C.F.R. §§1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT (\$)1,090.00**METHOD OF PAYMENT (check one)**1.  The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:Deposit Account Number: 02-4943

Deposit Account Number: \_\_\_\_\_

Charge Any Additional Fee Required Under 37 C.F.R. §1.16 and 1.17.  Charge the Issue Fee Set in 37 C.F.R. §1.18 at the Mailing of the Notice of Allowance.

**2. ■ Payment Enclosed: (CHECK #36934 & #36935)** Check     Money Order     Other**FEES CALCULATION****1. BASIC FILING FEE**

Large Entity Small Entity

| Fee Code            | Fee (\$) | Fee Code | Fee (\$) | Fee Description           | Fee Paid |
|---------------------|----------|----------|----------|---------------------------|----------|
| 101                 | 690      | 201      | 345      | Utility filing fee        | \$690.00 |
| 106                 | 310      | 206      | 155      | Design filing fee         | \$       |
| 107                 | 480      | 207      | 240      | Plant filing fee          | \$       |
| 108                 | 690      | 208      | 345      | Reissue filing fee        | \$       |
| 114                 | 150      | 214      | 75       | Provisional filing fee    | \$       |
| <b>SUBTOTAL (1)</b> |          |          |          | <b>(\$)</b> <b>690.00</b> |          |

**2. EXTRA CLAIM FEES**

|                    |    | Extra Claims | Fee from below | Fee Paid         |
|--------------------|----|--------------|----------------|------------------|
| Total claims       | 40 | -20** =      | 20             | x 18.00 = 360.00 |
| Independent Claims | 3  | -3** =       | x              | =                |

Multiple Dependent

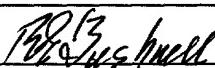
\*\* or number previously paid, if greater; For Reissues, see below

Large Entity Small Entity

| Fee Code            | Fee (\$) | Fee Code | Fee (\$) | Fee Description  |
|---------------------|----------|----------|----------|--|
| 103                 | 18       | 203      | 9        | Claims in excess of 20                                     |
| 102                 | 78       | 202      | 39       | Independent claims in excess of 3                          |
| 104                 | 260      | 204      | 130      | Multiple dependent claim, if not paid                      |
| 109                 | 78       | 209      | 39       | ** Reissue independent claims over original patent         |
| 110                 | 18       | 210      | 9        | ** Reissue claims in excess of 20 and over original patent |
| <b>SUBTOTAL (2)</b> |          |          |          | <b>(\$)</b> <b>360.00</b>                                  |

| Complete If Known                   |                       |          |          |  |                |
|-------------------------------------|-----------------------|----------|----------|--|----------------|
| Application Number                  | to be assigned        |          |          |  |                |
| Filing Date                         | 20 July 2000          |          |          |  |                |
| First Named Inventor                | KWANG-JIN YANG et al. |          |          |  |                |
| Examiner Name                       | to be assigned        |          |          |  |                |
| Group/Art Unit                      | to be assigned        |          |          |  |                |
| Attorney Docket No.                 | P56077                |          |          |  |                |
| FEE CALCULATION (continued)         |                       |          |          |  |                |
| 3. ADDITIONAL FEES                  |                       |          |          |  |                |
| Large Entity                        | Small Entity          |          |          |  |                |
| Fee Code                            | Fee (\$)              | Fee Code | Fee (\$) | Fee Description  | Fee Paid       |
| 105                                 | 130                   | 205      | 65       | Surcharge-late filing fee or oath  | \$             |
| 127                                 | 50                    | 227      | 25       | Surcharge-late provisional filing fee or cover sheet                       | \$             |
| 139                                 | 130                   | 139      | 130      | Non-English specification  | \$             |
| 147                                 | 2,520                 | 147      | 2,520    | For filing a request for reexamination                                     | \$             |
| 112                                 | 920*                  | 112      | 920*     | Requesting publication of SIR prior to Examiner action                     | \$             |
| 113                                 | 1,840*                | 113      | 1,840*   | Requesting publication of SIR after Examiner action                        | \$             |
| 115                                 | 110                   | 215      | 55       | Extension for reply within first month                                     | \$             |
| 116                                 | 380                   | 216      | 190      | Extension for reply within second month                                    | \$             |
| 117                                 | 870                   | 217      | 435      | Extension for reply within third month                                     | \$             |
| 118                                 | 1,360                 | 218      | 680      | Extension for reply within fourth month                                    | \$             |
| 128                                 | 1,850                 | 228      | 925      | Extension for reply within fifth month                                     | \$             |
| 119                                 | 300                   | 219      | 150      | Notice of Appeal   | \$             |
| 120                                 | 300                   | 220      | 150      | Filing a brief in support of an appeal                                     | \$             |
| 121                                 | 260                   | 221      | 130      | Request for oral hearing   | \$             |
| 138                                 | 1,510                 | 138      | 1,510    | Petition to institute a public use proceeding                              | \$             |
| 140                                 | 110                   | 240      | 55       | Petition to revive - unavoidable   | \$             |
| 141                                 | 1,210                 | 241      | 605      | Petition to revive - unintentional   | \$             |
| 142                                 | 1,210                 | 242      | 605      | Utility issue fee (or reissue)   | \$             |
| 143                                 | 430                   | 243      | 215      | Design issue fee   | \$             |
| 144                                 | 580                   | 244      | 290      | Plant issue fee  | \$             |
| 122                                 | 130                   | 122      | 130      | Petitions to the Commissioner  | \$             |
| 123                                 | 50                    | 123      | 50       | Petitions related to provisional applications                              | \$             |
| 126                                 | 240                   | 126      | 240      | Submission of Information Disclosure Statement                             | \$             |
| 581                                 | 40                    | 581      | 40       | Recording each patent assignment per property (Times number of properties) | \$ 40.00       |
| 146                                 | 690                   | 246      | 345      | Filing a submission after final rejection (37 C.F.R. §1.129(a))            | \$             |
| 149                                 | 690                   | 249      | 345      | For each additional invention to be examined (37 C.F.R. §1.129(b))         | \$             |
| Other Fee (specify) _____           |                       |          |          |  | \$             |
| Other Fee (specify) _____           |                       |          |          |  | \$             |
| ** Reduced by Basic Filing Fee Paid |                       |          |          | <b>SUBTOTAL (3)</b>  | <b>\$40.00</b> |

**SUBMITTED BY****Complete (if applicable)**

|                       |   |      |              |                         |        |
|-----------------------|---|------|--------------|-------------------------|--------|
| Typed or Printed Name | Robert E. Bushnell, Esq.  |      |              | Reg. Number             | 27,774 |
| Signature             |  | Date | 20 July 2000 | Deposit Account User ID |        |

REB/sb

1                   **TITLE OF THE INVENTION**

2                   **BIT-RATE INDEPENDENT OPTICAL RECEIVER AND METHOD**

3                   **THEREOF**

4                   **CLAIM OF PRIORITY**

This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. §119 from an application for *AN OPTICAL RECEIVERS WITH BIT-RATE INDEPENDENT CLOCK AND DATA RECOVERY AND METHOD THEREFOR* earlier filed in the Korean Industrial Property Office on the 5<sup>th</sup> of August 1999 and there duly assigned Serial No. 32170/1999.

5                   **BACKGROUND OF THE INVENTION**

6                   **Technical Field**

7                   The present invention relates generally to an optical receiver for converting an input optical  
8                   signal to an electrical signal for data recovery and a method thereof in an optical transmission  
9                   system.

1

## Related Art

2       A variety of protocols are available to an optical transmission system, such as protocols for  
3       fiber distributed data interface (FDDI), enterprise systems connectivity (ESCON), fiber channel,  
4       gigabit Ethernet, and asynchronous transfer mode (ATM). Various bit rates are used for the  
5       protocols, including 125 megabits per second (Mbps), 155 Mbps, 200 Mbps, 622 Mbps, 1062 Mbps,  
6       1.25 gigabits per second (Gbps), and 2.5 Gbps.

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7       Among the protocols and bit rates, an optical transmission system selects an appropriate  
8       protocol/bit rate. Since the bit rate of an optical signal is preset in the optical transmission system,  
9       an optical receiver in a relay or a terminal operates at the bit rate according to the selected protocol.  
10      The bit rate corresponds to a transmission rate. The bit rate can be expressed as a transmission rate  
11     of a number of bits per second (bps).

12  
13      I have found that it would be desirable to improve optical receiver technology. Efforts have  
been made to improve optics-related technologies.

14      Exemplars of recent efforts in the art include U.S. Serial No. 09/484,061 for *METHOD AND*  
15     *APPARATUS FOR IDENTIFYING BIT RATE* applied for by Yang, U.S. Patent No. 5,181,134 for  
16     *A Photonic Cross-Connect Switch* issued to Fatehi et al., U.S. Patent No. 4,888,791 for *A Clock*  
17     *Decoder and Data Bit Transition Detector for Fiber Optic Work Station* issued to Barndt, Sr., U.S.

1 Patent No. 5,510,919 for *An Optical System for Transmitting a Multilevel Signal* issued to Wedding,  
2 U.S. Patent No. 5,144,469 for *A Method for the Transmission of Data Between Two Stations by*  
3 *Means of Optical Waveguides* issued to Brahms et al., U.S. Patent No. 5,550,864 for *A Bit Rate-*  
4 *Insensitive Mechanism for Transmitting Integrated Clock and Data Signals over Digital*  
5 *Communication Link* issued to Toy et al., U.S. Patent No. 4,524,462 for *A System for Jointly*  
6 *Transmitting High-Frequency and Low-Frequency Digital Signals over a Fiber-Optical Carrier*  
7 issued to Cottatelucci, U.S. Patent No. 6,069,722 for *A Transmitter for Optically Transmitting*  
8 *Analog Electric Signals, and Digital Transmission System* issued to Schlag, U.S. Patent No.  
9 6,034,801 for *A Transmitting Device, Transmitting Apparatus and Optical Transmission System for*  
10 *Optically Transmitting Analog Electrical Signals* issued to Pfeiffer, and U.S. Patent No. 4,475,212  
11 for *A Frequency-Independent, Self-Clocking Encoding Technique and Apparatus for Digital*  
12 *Communications* issued to McLean et al..

13 While these recent efforts provide advantages, I note that they fail to adequately provide an  
improved bit-rate independent optical receiver and method thereof having enhanced efficiency.

15 **SUMMARY OF THE INVENTION**

16 It is, therefore, an object of the present invention to provide a bit-rate independent optical  
17 receiver for accommodating optical signals at different bit rates and a method thereof.

18 It is another object of the present invention to provide a bit-rate independent optical receiver

1 for recovering data and clock signals from optical signals received at different bit rates, and a method  
2 thereof.

3 It is a further object of the present invention to provide a bit-rate independent optical receiver  
4 and a method thereof, which can increase transmission quality and a transmission distance.

5 These and other objects can be achieved by providing a bit-rate independent optical receiver.

6 In the bit-rate independent optical receiver, an optoelectric converter converts an input optical signal  
7 to an original electrical signal, a bit rate identifying unit performs an exclusive-OR (XOR) logic  
8 operation upon the original electrical signal received from the optoelectric converter and a second  
9 signal corresponding to the original electrical signal delayed by a predetermined time, and detects  
10 a bit rate from the resultant signal resulting from the exclusive-OR logic operation, a reference clock  
11 generator generates a reference clock signal according to the detected bit rate, and a clock and data  
12 recovery circuit recovers a clock signal and data from the input signal according to the reference  
13 clock signal.

14 To achieve these and other objects in accordance with the principles of the present invention,  
15 as embodied and broadly described, the present invention provides a bit-rate independent optical  
16 receiver comprising: an optoelectric converter for converting an input optical signal to an electrical  
17 signal; a bit rate identifying unit having a identification signal generator for delaying the input signal,

1 comparing the delayed signal with the original input signal period by period, and generating a  
2 sensing signal, and a bit rate deriving unit for loss-pass-filtering the sensing signal and determining  
3 the bit rate from the resulting voltage level; a reference clock generator having a plurality of  
4 oscillators for generating clock signals of different frequencies, for selectively operating the  
5 oscillators to generate the reference clock signal the same as the bit rate detected by the bit rate  
6 identifying unit; and a clock and data recovery circuit for recovering a clock signal and data from  
7 the input signal according to the reference clock signal.

To achieve these and other objects in accordance with the principles of the present invention, as embodied and broadly described, the present invention provides an apparatus, comprising: a converter converting an input optical signal to an original electrical signal; an identification unit receiving said original electrical signal, generating a first signal corresponding to said original electrical signal delayed by a predetermined quantity of time, generating a second signal corresponding to said original electrical signal not delayed, comparing said first and second signals, forming a third signal in dependence upon said comparing of said first and second signals, detecting a bit rate in dependence upon said third signal; a clock generator generating a reference clock signal in dependence upon said detected bit rate; and a recovery unit recovering an input clock signal and data from said input optical signal in dependence upon said reference clock signal.

To achieve these and other objects in accordance with the principles of the present invention,

1 as embodied and broadly described, the present invention provides a method of operating a receiver  
2 which functions independently of a bit rate of a received signal, comprising: receiving an original  
3 signal; generating a resultant signal by comparing a first signal and a second signal, said first signal  
4 corresponding to said original signal delayed by a predetermined quantity of time, said second signal  
5 corresponding to said original signal not delayed; determining a bit rate of said original signal in  
6 dependence upon said resultant signal; generating a reference clock signal in dependence upon said  
7 determined bit rate; and recovering an input clock signal and data from said original signal in  
8 dependence upon said reference clock signal.

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14 To achieve these and other objects in accordance with the principles of the present invention,  
15 as embodied and broadly described, the present invention provides an apparatus, comprising: a  
16 converter converting an input optical signal to an original electrical signal; an identification unit  
17 receiving said original electrical signal, generating a first signal corresponding to said original  
18 electrical signal delayed by a predetermined quantity of time, generating a second signal corresponding  
to said original electrical signal not delayed, forming a third signal by performing an exclusive-OR  
logic operation upon said first and second signals, detecting a bit rate in dependence upon said third  
signal; a clock generator generating a reference clock signal in dependence upon said detected bit  
rate; and a recovery unit recovering an input clock signal and data from said input optical signal in  
dependence upon said reference clock signal.

1 The present invention is more specifically described in the following paragraphs by reference  
2 to the drawings attached only by way of example. Other advantages and features will become  
3 apparent from the following description and from the claims.

## BRIEF DESCRIPTION OF THE DRAWINGS

5 In the accompanying drawings, which are incorporated in and constitute a part of this  
6 specification, embodiments of the invention are illustrated, which, together with a general  
7 description of the invention given above, and the detailed description given below, serve to  
8 exemplify the principles of this invention.

FIG. 1 is a schematic block diagram of an optical receiver;

FIG. 2 is a block diagram of an optical receiver according to an embodiment of the present invention, in accordance with the principles of the present invention;

FIG. 3 is a block diagram of a bit rate identifying unit shown in FIG. 2, in accordance with the principles of the present invention;

14 FIGs. 4A and 4B are exemplary waveforms output from function blocks, for describing the  
15 operation of the bit rate identifying unit shown in FIG. 3, in accordance with the principles of the  
16 present invention; and

17 FIG. 5 is graph showing the relationship between the bit rate of an optical signal versus the  
18 output direct current (DC) level of a filter shown in FIG. 3, in accordance with the principles of the  
19 present invention.

1                   **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

2                   While the present invention will be described more fully hereinafter with reference to the  
3                   accompanying drawings, in which a preferred embodiment of the present invention is shown, it is  
4                   to be understood at the outset of the description which follows that persons of skill in the appropriate  
5                   arts may modify the invention here described while still achieving the favorable results of this  
6                   invention. Accordingly, the description which follows is to be understood as being a broad, teaching  
7                   disclosure directed to persons of skill in the appropriate arts, and not as limiting upon the present  
invention.

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10                  FIG. 1 is a schematic block diagram of an optical receiver. Referring to FIG. 1, the optical  
11                  receiver is comprised of an optoelectric (O/E) converter 10, an amplifier (AMP) 20 for amplifying  
12                  an electrical signal outputted from the optoelectric converter 10, a clock generator 40 for generating  
13                  a reference clock signal according to the bit rate of an input optical signal, and a clock and data  
14                  recovery (CDR) circuit 30 for recovering a clock signal and data from an amplified signal received  
from the amplifier 20.

15                  An optical signal is input to the optoelectric converter 10 at a bit rate preset according to a  
16                  single protocol used in a corresponding optical transmission system. Therefore, the optical receiver  
17                  receives an optical signal at the single bit rate. The clock and data recovery circuit 30 receives a

1       clock signal of a predetermined single frequency according to the bit rate from the clock generator  
2       40 and recovers data and a clock signal from the input signal based on the single reference clock  
3       signal by reshaping, regeneration, and retiming.

4                   Optical communication systems are being developed from a time division multiplexing  
5       (TDM) to a wavelength division multiplexing (WDM). The wavelength division multiplexing  
6       scheme multiplexes a plurality of channels at different wavelengths and propagates the multiplexed  
7       optical signals onto a single optical fiber. Accordingly, research has been conducted on a  
multiplexing of optical signals in different channels with different protocols and bit rates into one  
strand of optical fiber. Due to an increasing demand for optical transmission systems and the  
increase of data traffic especially in metropolitan areas, a wavelength division multiplexing system  
for use in metropolitan areas should be flexible enough to accommodate various formats for fiber  
distributed data interface (FDDI), enterprise systems connectivity (ESCON), fiber channel, gigabit  
Ethernet, and asynchronous transfer mode (ATM), which mainly deal with data traffic, as well as  
those for synchronous digital hierarchy/synchronous optical network (SDH/SONET) evolved from  
14      voice transmission.

16                  In this context, a so-called protocol free system has been developed to accommodate optical  
signals at different bit rates. Therefore, optical signals are recovered just by waveform shaping, that  
17       is, reshaping and regeneration, without recovering a clock signal. The resulting noise and timing  
18

1 jitters increased as an optical signal passes through nodes decreases transmission quality. In  
2 particular, a receiver or transponder confined to the reshaping and regeneration function is limited  
3 in transmission distance due to the decreased transmission quality when various protocols/bit rates  
4 are used in an optical network.

5 A preferred embodiment of the present invention will be described hereinbelow with  
6 reference to the accompanying drawings. In the following description, well-known functions or  
7 constructions are not described in detail since they would obscure the invention in unnecessary  
8 detail.

An optical receiver according to the present invention receives optical signals at different bit rates from remote optical transmission systems and detects the bit rates of the received optical signals. It also recovers the received signals through retiming using clock signals having the same bit rate with the input data extracted from the received optical signals.

13 FIG. 2 is a block diagram of an optical receiver according to an embodiment of the present  
14 invention. The optical receiver is a protocol-free one independent of a bit rate and can operate with  
15 an optical signal received at any bit rate. The optical receiver operates independently of the input  
16 signal's bit rate. The optical receiver is insensitive to bit rate. The optical receiver is transparent to  
17 signal bit rate.

1 Referring to FIG. 2, the optical receiver includes the optoelectric converter 10 for converting  
2 an optical signal received at any bit rate to an electrical signal, the amplifier 20 for amplifying the  
3 electrical signal outputted from the optoelectric converter 10, a bit rate identifying unit 50 for  
4 identifying a bit rate from the received signal, a reference clock generator 60 for generating a  
5 reference clock signal according to the identified bit rate, and a clock and data recovery circuit 70  
6 for recovering a clock signal and data from the amplified signal received from the amplifier 20 by  
7 means of the reference clock signal generated from the reference clock generator 60.

8 Since the optical signal inputted to the optoelectric converter 10 is very weak, because the  
9 signal reaches the corresponding receiver after being transmitted a long distance, the amplifier 20  
10 is included to amplify this input signal to an appropriate level.

11 An optical signal is applied at a certain bit rate in a certain protocol to the input of the  
12 optoelectric converter 10. The input optical signal is converted to an electrical signal by the  
13 optoelectric converter 10 and its bit rate is identified by the bit rate identifying unit 50. The  
14 reference clock generator 60 includes a plurality of oscillators for generating clock signals with  
15 different frequencies, which is different than the clock generator 40 shown in Fig. 1. The clock  
16 generator 40 in Fig. 1 only generates a single type of clock signal, in accordance with the single bit  
17 rate of the input optical signal, as shown in Fig. 1. However, the reference clock generator 60  
18 selectively operates the internal oscillators to generate a reference clock signal at a detected bit rate.

1 The clock and data recovery circuit 70 is a programmable circuit, which is different than the clock  
2 and data recovery circuit 30 shown in Fig. 1, for reshaping, regeneration, and retiming of an input  
3 signal according to the reference clock signal received from the reference clock generator 60.

4 For reference, XOR-gating two particular signals is the equivalent of performing an  
5 exclusive-OR logic operation upon those two particular signals. The bit rate identifying unit 50  
6 identifies the bit rate of an input signal from a signal delayed from the input signal by a  
7 predetermined time and a voltage level produced by XOR-gating the input signal with the delayed  
8 signal and then low-pass-filtering the XOR-gated signal. A bit rate identifying unit has been  
9 described in U.S. Serial No. 09/484,061 entitled "Method and apparatus for identification of bit rate,"  
10 here incorporated by reference. The structure and operation of the bit rate identifying unit 50 will  
11 be described in detail referring to the attached drawings.

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FIG. 3 is a block diagram of the bit rate identifying unit shown in FIG. 2 and FIGs. 4A and  
4B shows signals outputted from function blocks, for describing the operation of the bit rate  
identifying unit shown in FIG. 3. Referring to FIGs. 3, 4A, and 4B, the bit rate identifying unit 50  
includes an identification signal generator 40a for delaying an input signal by a long time period,  
comparing the original signal with the delayed signal period by period, and generating a sensing  
signal, and a bit rate deriving unit 40b for determining a bit rate of the received signal from a voltage  
level obtained by low-pass-filtering the identification signal.

1       The identification signal generator 40a includes a buffer 41 for duplicating an input signal  
2       into two signals equal to the input signal, a delay 42 for delaying one of the buffer outputs by a  
3       predetermined time, and an operator 43 for performing the exclusive-OR (XOR) operation upon the  
4       delayed signal and the original input signal, and generating a bit rate identification signal.

5                  With reference to Fig. 4A, in the thus-constituted bit rate identification signal generator 40a,  
6       the delay 42 generates a signal (b) delayed from an input signal (a) by a predetermined time D, for  
7       the input of the signal (a) with pulse period 2T. Here, D is T/2 for example. The operator 43  
8       generates a sensing signal (c) by XOR-gating the input signal (a) with the delayed signal (b). The  
9       sensing signal (c) has a plurality of pulses with high level periods presented at the same intervals as  
10      D. For example, at a first moment in time, if original input signal (a) corresponds to a 0 and delayed  
11      signal (b) also corresponds to a 0, then the resulting sensing signal (c) will be a 0 due to the logical  
12      exclusive-OR gate operation performed upon signals (a) and (b). At a second moment in time, if  
13      signal (a) is a 0 and signal (b) is a 1, then the signal (c) will be a 1 due to the logical exclusive-OR  
14      gate operation. At a third moment in time, if signal (a) is a 1 and signal (b) is a 0, then signal (c) will  
15      be a 1. At a fourth moment in time, if signal (a) is a 1 and signal (b) is also a 1, then signal (c) will  
16      be a 0.

17                  Meanwhile, FIG. 4B illustrates an input signal (a) at a different bit rate from that of the input  
18      signal (a) shown in FIG. 4A. In FIG. 4B, the bit rate of the input signal (a) is a fourth of that of the

1 input signal (a) shown in FIG. 4A, that is, the input signal (a) has pulse period T four times greater  
2 than T. The delay 42 generates a signal (b) delayed from the input signal (a) by  $D = T/2$ , namely,  
3  $T/8$ . The operator 43 EXOR-gates the input signal (a) with the delayed signal (b) and generates  
4 a sensing signal (c). The sensing signal (c) has a plurality of pulses with high level periods  
5 presented at the same intervals as D.

6 In comparison between FIGs. 4A and 4B, when the sensing signals are generated using input  
7 signals received for the same time period, the pulses of the sensing signal (c) are a few times more  
8 than those of the sensing signal (c). That is, the pulse numbers of the sensing signals are different  
9 due to the different bit rates of the input signals, and the difference between the pulse numbers is  
10 proportional to the difference between the bit rates.  
11  
12

13 Therefore, a bit rate can be detected by checking the number of pulses of a sensing signal  
14 generated for a predetermined time. However, such a circuit as can directly count the pulses of the  
15 sensing signal to detect the bit rate of the input signal is difficult to configure since the current  
16 optical transmission system employs a maximum bit rate in Gbps units.  
17

18 To overcome this limitation, the bit rate deriving unit 40b low-pass-filters the sensing signal  
19 and detects the bit rate from the resulting voltage level. Returning to FIG. 3, the bit rate deriving  
20 unit 40b includes a filter 44 for low-pass filtering a sensing signal received from the operator 43 of  
21

1 the identification signal generator 40a, an analog-to-digital converter (ADC) 45 for converting an  
2 analog signal received from the filter 44 to a digital signal, and a determiner 46 for determining the  
3 bit rate from the output of the analog-to-digital converter 45.

4 The filter 44 shown in FIG. 3 is a low pass filter. The filter 44 receives a high frequency  
5 digital signal and outputs direct voltage components having levels according to the pulses of the  
6 inputted digital signal. That is, the signal outputted from the filter 44 can be regarded as an analog  
7 signal. The analog-to-digital converter 45 converts the direct voltage components into digital values  
8 as a step prior to determining the direct voltage level of the inputted analog signal.

9  
10 FIG. 5 is a graph showing the relationship between an optical signal bit rate and the output  
11 level of the filter 44 shown in FIG. 3. In FIG. 5, the voltage levels of a sensing signal low-pass-  
12 filtered in the filter 44 are shown with respect to bit rates ranging from 100 Mbps to 2.5 Gbps. As  
13 shown in FIG. 5, since the voltage level increases linearly with the bit rate, the bit rate can be  
determined from the voltage level.

14 By use of the bit rate identifying unit 50, the reference clock generator 60, and the clock and  
15 data recovery circuit 70, the optical receiver of the present invention can detect a bit rate from an  
16 optical signal at the bit rate received from an optical transmission system.

1 As described above, the bit-rate independent optical receiver of the present invention detects  
2 a bit rate from an optical signal received at the bit rate in recovering the input signal. Therefore, it  
3 can accommodate optical signals at different bit rates and recover data and a clock signal from an  
4 input optical signal, thereby increasing transmission quality and a transmission distance.

5 Furthermore, the optical receiver can operate adaptively to a bit rate. Especially, when the  
6 optical receiver is applied to a wavelength division multiplexing transmission system together with  
7 other devices operated at different bit rates, there is no need for changing a channel card in the  
8 optical receiver even if wavelengths assigned to the devices or a system structure should be changed.

9 While the present invention has been illustrated by the description of embodiments thereof,  
10 and while the embodiments have been described in considerable detail, it is not the intention of the  
11 applicant to restrict or in any way limit the scope of the appended claims to such detail. Additional  
12 advantages and modifications will readily appear to those skilled in the art. Therefore, the invention  
13 in its broader aspects is not limited to the specific details, representative apparatus and method, and  
14 illustrative examples shown and described. Accordingly, departures may be made from such details  
without departing from the spirit or scope of the applicant's general inventive concept.

**What is claimed is:**

1        1. An apparatus, comprising:

2              a converter converting an input optical signal to an original electrical signal;

3              an identification unit receiving said original electrical signal, generating a first signal

4              corresponding to said original electrical signal delayed by a predetermined quantity of time, generating

5              a second signal corresponding to said original electrical signal not delayed, comparing said first and

6              second signals, forming a third signal in dependence upon said comparing of said first and second

signals, detecting a bit rate in dependence upon said third signal;

7              a clock generator generating a reference clock signal in dependence upon said detected bit  
rate; and

8              a recovery unit recovering an input clock signal and data from said input optical signal in  
dependence upon said reference clock signal.

9        2. The apparatus of claim 1, said apparatus corresponding to an optical receiver

10      receiving optical signals having a plurality of different bit rates.

11        3. The apparatus of claim 1, said bit rate of said input optical signal corresponding to

12      a transmission rate.

1           4. The apparatus of claim 1, further comprising an amplifier amplifying said original  
2 electrical signal received from said converter.

1           5. The apparatus of claim 4, said amplifier outputting said amplified electrical signal  
2 to said identification unit.

1           6. The apparatus of claim 1, said converter corresponding to an optoelectric converter.

1           7. The apparatus of claim 1, said identification unit corresponding to a bit rate  
identification unit.

1           8. The apparatus of claim 1, said comparing performed by said identification unit  
corresponding to said identification unit performing an exclusive-OR logic operation upon said first  
and second signals.

1           9. The apparatus of claim 8, said forming of said third signal performed by said  
2 identification unit corresponding to said identification unit forming said third signal in dependence  
3 upon said exclusive-OR logic operation performed upon said first and second signals.

1           10. The apparatus of claim 9, said identification unit comprising:

2           a first unit delaying said original electrical signal, performing said exclusive-OR operation  
3           upon said first and second signals, and forming said third signal; and  
4           a second unit filtering said third signal, detecting said bit rate in dependence upon a voltage  
5           level of said filtered third signal.

1           11.      The apparatus of claim 10, said filtering corresponding to low-pass filtering.

1           12.      The apparatus of claim 10, said first unit corresponding to a bit rate identification  
2           signal generator.

1           13.      The apparatus of claim 10, said second unit corresponding to a bit rate deriving unit.

1           14.      The apparatus of claim 10, said second unit comprising:

2           a filter filtering said third signal;

3           an analog-to-digital converter receiving said filtered third signal, converting said filtered third

4           signal from an analog signal to a digital signal; and

5           a determiner determining said bit rate in dependence upon said digital signal received from

6           said analog-to-digital converter.

1        15. The apparatus of claim 10, said first unit comprising:

2              a buffer unit receiving said original electrical signal, outputting two duplicate signals  
3              substantially equivalent to said original electrical signal, said two duplicate signals corresponding  
4              to a primary signal and a secondary signal;

5              a delay unit receiving said primary signal, delaying said primary signal by said predetermined  
6              quantity of time, outputting said primary signal, said delayed primary signal corresponding to said  
7              first signal; and

8              an operator unit performing said exclusive-OR logic operation upon said first and second  
signals.

1        16. The apparatus of claim 1, said clock generator comprising a plurality of oscillators  
2              generating clocking signals of different frequencies and selectively operating said oscillators to  
3              generate said reference clock signal in dependence upon said bit rate detected by said identification  
4              unit.

1        17. A method of operating a receiver which functions independently of a bit rate of a  
2              received signal, comprising:

3              receiving an original signal;

4              generating a resultant signal by comparing a first signal and a second signal, said first signal  
5              corresponding to said original signal delayed by a predetermined quantity of time, said second signal

6        corresponding to said original signal not delayed;  
7                determining a bit rate of said original signal in dependence upon said resultant signal;  
8                generating a reference clock signal in dependence upon said determined bit rate; and  
9                recovering an input clock signal and data from said original signal in dependence upon said  
10          reference clock signal.

1                18.      The method of claim 17, said comparing of said first and second signals  
2        corresponding to performing an exclusive-OR logic operation upon said first and second signals, said  
3        resultant signal being generated as a result of said exclusive-OR logic operation.

1                19.      The method of claim 18, further comprising:  
2                said original signal corresponding to an input optical signal;  
3                converting said input optical signal to an electrical signal;  
4                outputting two duplicate signals substantially equivalent to said electrical signal, said two  
5        duplicate signals corresponding to a primary signal and a secondary signal; and  
6                delaying said primary signal by said predetermined quantity of time, outputting said primary  
7        signal, said delayed primary signal corresponding to said first signal.

1                20.      The method of claim 17, said first, second, and third signals corresponding to  
2        electrical signals.

1           21. The method of claim 17, said method corresponding to receiving signals having a  
2         plurality of different bit rates.

1           22. The method of claim 17, said original signal received corresponding to a plurality of  
2         original signals received, said recovering of said input clock signal and data from said original signal  
3         being performed for said plurality of original signals received, said plurality of original signals  
4         received having a respective plurality of different bit rates.

1           23. The method of claim 17, said recovering of said input clock signal and data from said  
2         original signal being performed for a plurality of original signals received, said plurality of original  
3         signals received having a respective plurality of different bit rates.

1           24. The method of claim 17, said method corresponding to receiving optical signals  
2         having a plurality of different bit rates.

1           25. The method of claim 17, further comprising:  
2         receiving an input optical signal;  
3         converting said input optical signal to an original electrical signal;  
4         outputting two duplicate signals substantially equivalent to said original electrical signal, said

5 two duplicate signals corresponding to a primary signal and a secondary signal; and  
6 delaying said primary signal by said predetermined quantity of time, outputting said primary  
7 signal, said delayed primary signal corresponding to said first signal.

1 26. The method of claim 17, further comprising:

2 said receiving of said original signal being performed by an optoelectric converter, said  
3 original signal being an optic signal, said optoelectric converter converting said original optic signal  
4 to an electrical signal;

5 outputting two duplicate signals substantially equivalent to said electrical signal, said two  
6 duplicate signals corresponding to a primary signal and a secondary signal, said outputting of said  
7 two duplicate signals being performed by a buffer; and

8 delaying said primary signal by said predetermined quantity of time, outputting said primary  
signal, said delayed primary signal corresponding to said first signal.

1 27. The method of claim 17, said generating of said reference clock signal being

2 performed by a clock generator, said clock generator comprising a plurality of oscillators generating  
3 clocking signals of different frequencies and selectively operating said oscillators to generate said  
4 reference clock signal in dependence upon said detected bit rate.

1 28. An apparatus, comprising:

2           a converter converting an input optical signal to an original electrical signal;  
3           an identification unit receiving said original electrical signal, generating a first signal  
4        corresponding to said original electrical signal delayed by a predetermined quantity of time, generating  
5        a second signal corresponding to said original electrical signal not delayed, forming a third signal  
6        by performing an exclusive-OR logic operation upon said first and second signals, detecting a bit  
7        rate in dependence upon said third signal;

8           a clock generator generating a reference clock signal in dependence upon said detected bit  
9        rate; and

10           a recovery unit recovering an input clock signal and data from said input optical signal in  
11        dependence upon said reference clock signal.

12           29.       The apparatus of claim 28, said clock generator comprising a plurality of oscillators  
13        generating clocking signals of different frequencies and selectively operating said oscillators to  
14        generate said reference clock signal in dependence upon said bit rate detected by said identification  
15        unit.

16           30.       The apparatus of claim 28, said input optical signal corresponding to a plurality of  
17        input optical signals, said recovering of said input clock signal and data from said input optical  
18        signal being performed for each of said plurality of input optical signals, said plurality of input  
19        optical signals received having a plurality of different bit rates.

1       31. The apparatus of claim 30, said converter corresponding to an optoelectric converter.

1       32. The apparatus of claim 31, said identification unit corresponding to a bit rate  
2       identification unit.

1       33. The apparatus of claim 32, said identification unit comprising:  
2              a first unit delaying said original electrical signal, performing said exclusive-OR operation  
3              upon said first and second signals, and forming said third signal; and  
4              a second unit filtering said third signal, detecting said bit rate in dependence upon a voltage  
5              level of said filtered third signal.

1       34. The apparatus of claim 33, said second unit comprising:  
2              a filter filtering said third signal;  
3              an analog-to-digital converter receiving said filtered third signal, converting said filtered third  
4              signal from an analog signal to a digital signal; and  
5              a determiner determining said bit rate in dependence upon said digital signal received from  
6              said analog-to-digital converter.

1       35. The apparatus of claim 33, said first unit comprising:

2           a buffer unit receiving said original electrical signal, outputting two duplicate signals  
3           substantially equivalent to said original electrical signal, said two duplicate signals corresponding  
4           to a primary signal and a secondary signal;  
5           a delay unit receiving said primary signal, delaying said primary signal by said predetermined  
6           quantity of time, outputting said primary signal, said delayed primary signal corresponding to said  
7           first signal; and  
8           an operator unit performing said exclusive-OR logic operation upon said first and second  
9           signals.

36.       The apparatus of claim 33, said clock generator comprising a plurality of oscillators generating clocking signals of different frequencies and selectively operating said oscillators to generate said reference clock signal in dependence upon said bit rate detected by said identification unit.

1           37.      The apparatus of claim 33, said filtering corresponding to low-pass filtering.

1           38.      The apparatus of claim 37, said second unit comprising:

2           a filter filtering said third signal;

3           an analog-to-digital converter receiving said filtered third signal, converting said filtered third  
4           signal from an analog signal to a digital signal; and

5           a determiner determining said bit rate in dependence upon said digital signal received from  
6        said analog-to-digital converter.

1           39.     The apparatus of claim 38, said first unit comprising:

2           a buffer unit receiving said original electrical signal, outputting two duplicate signals  
3        substantially equivalent to said original electrical signal, said two duplicate signals corresponding  
4        to a primary signal and a secondary signal;

5           a delay unit receiving said primary signal, delaying said primary signal by said predetermined  
6        quantity of time, outputting said primary signal, said delayed primary signal corresponding to said  
7        first signal; and

8           an operator unit performing said exclusive-OR logic operation upon said first and second  
9        signals.

10          40.     The apparatus of claim 39, said clock generator comprising a plurality of oscillators  
11        generating clocking signals of different frequencies and selectively operating said oscillators to  
12        generate said reference clock signal in dependence upon said bit rate detected by said identification  
13        unit.

## **ABSTRACT OF THE DISCLOSURE**

A bit-rate independent optical receiver and a method thereof. In the bit-rate independent optical receiver, an optoelectric converter converts an input optical signal to an original electrical signal, a bit rate identifying unit forms a resultant signal by performing an exclusive-OR (XOR) logic operation on the original electrical signal received from the optoelectric converter and a second signal corresponding to the original electrical signal delayed by a predetermined quantity of time, and detects a bit rate from the resultant signal, a reference clock generator generates a reference clock signal according to the detected bit rate, and a clock and data recovery circuit recovers a clock signal and data from the input signal according to the reference clock signal.

FIG. 1

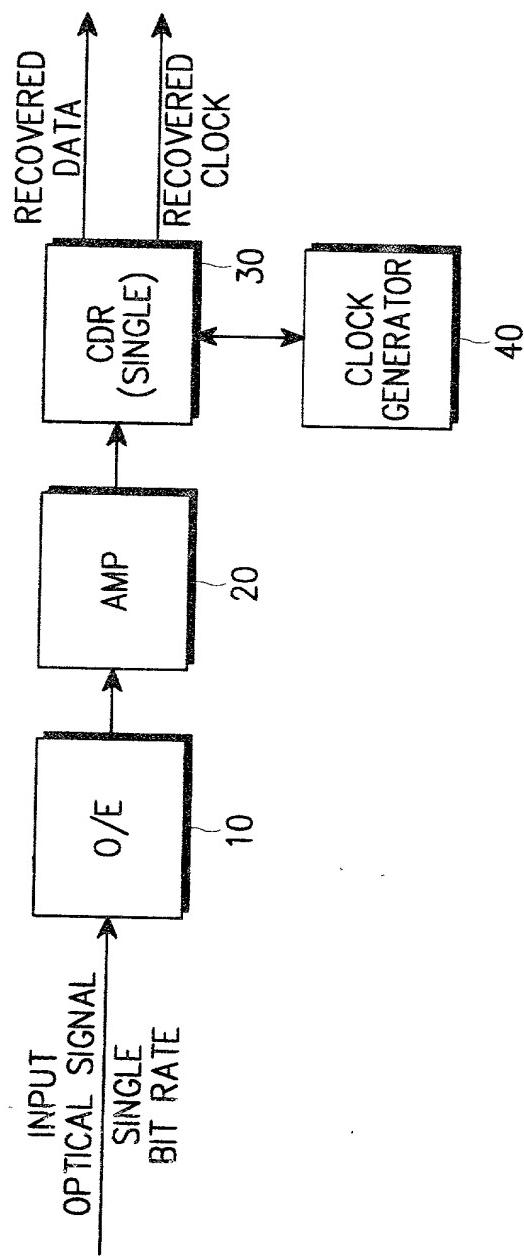


FIG. 2

2/6

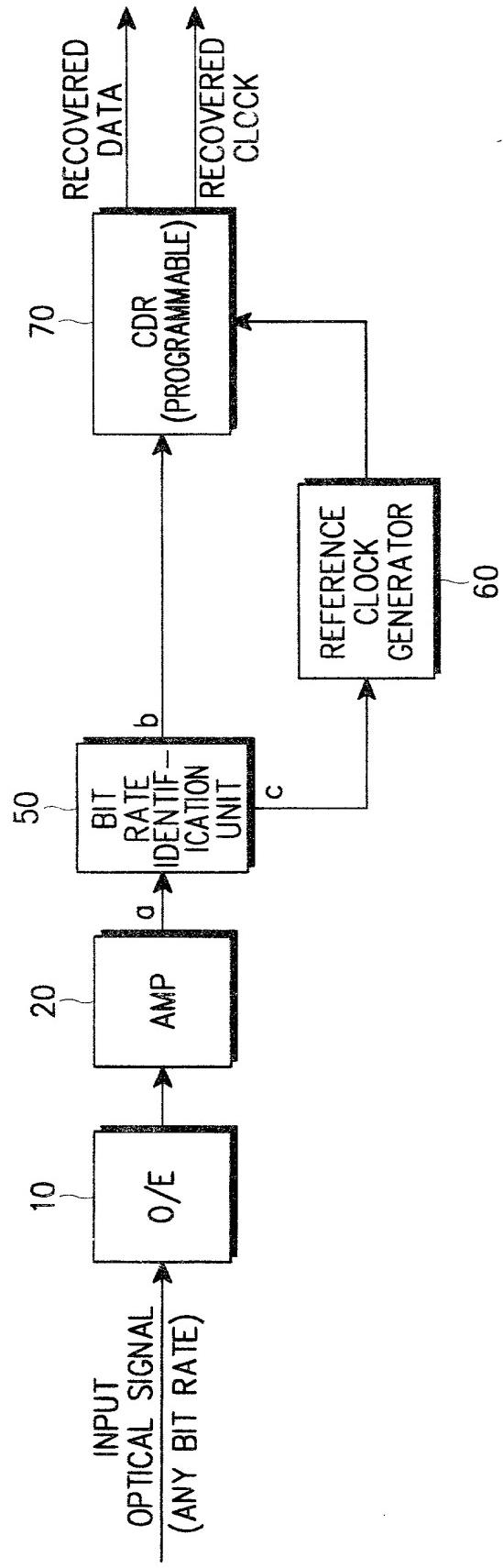


FIG. 3

3/6

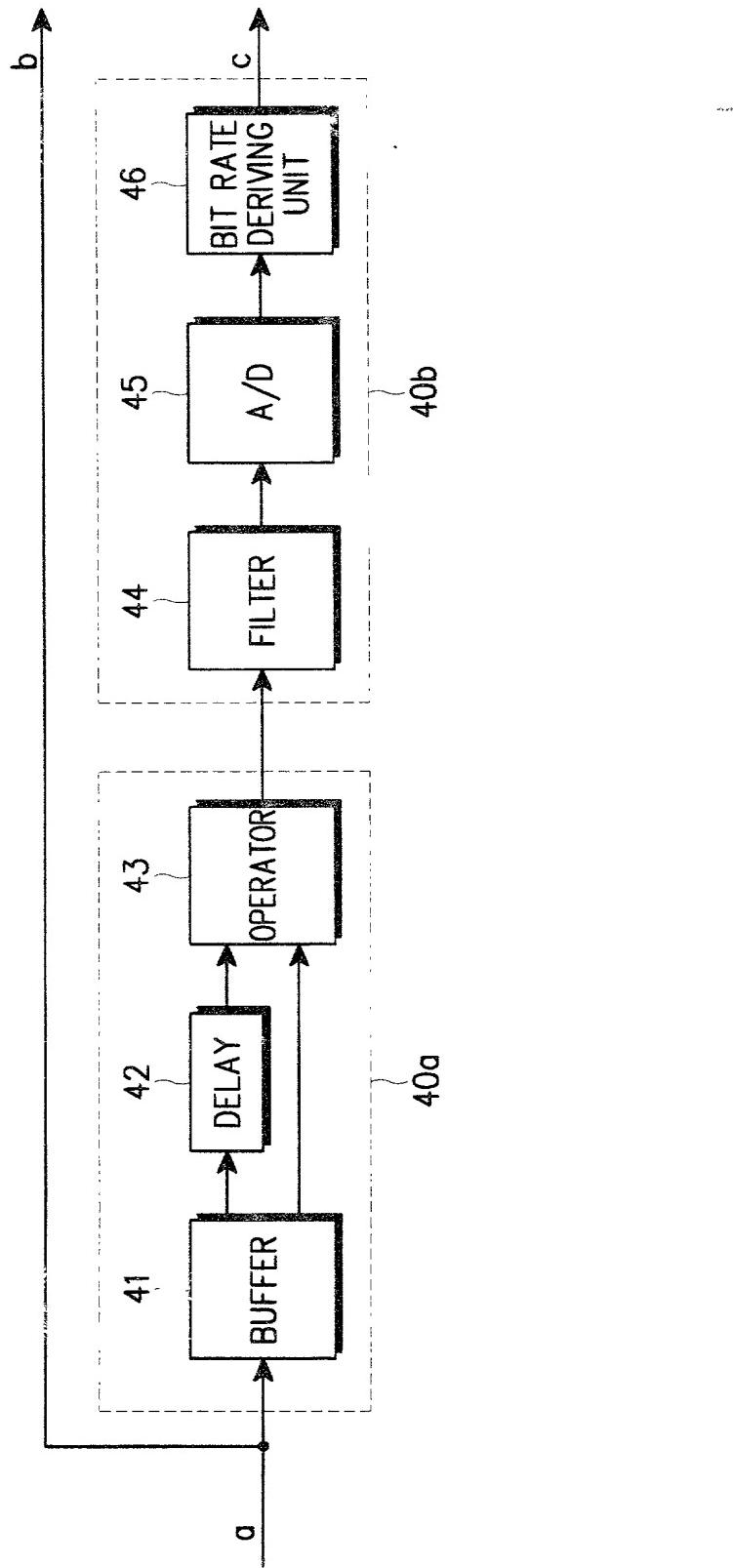


FIG. 4A

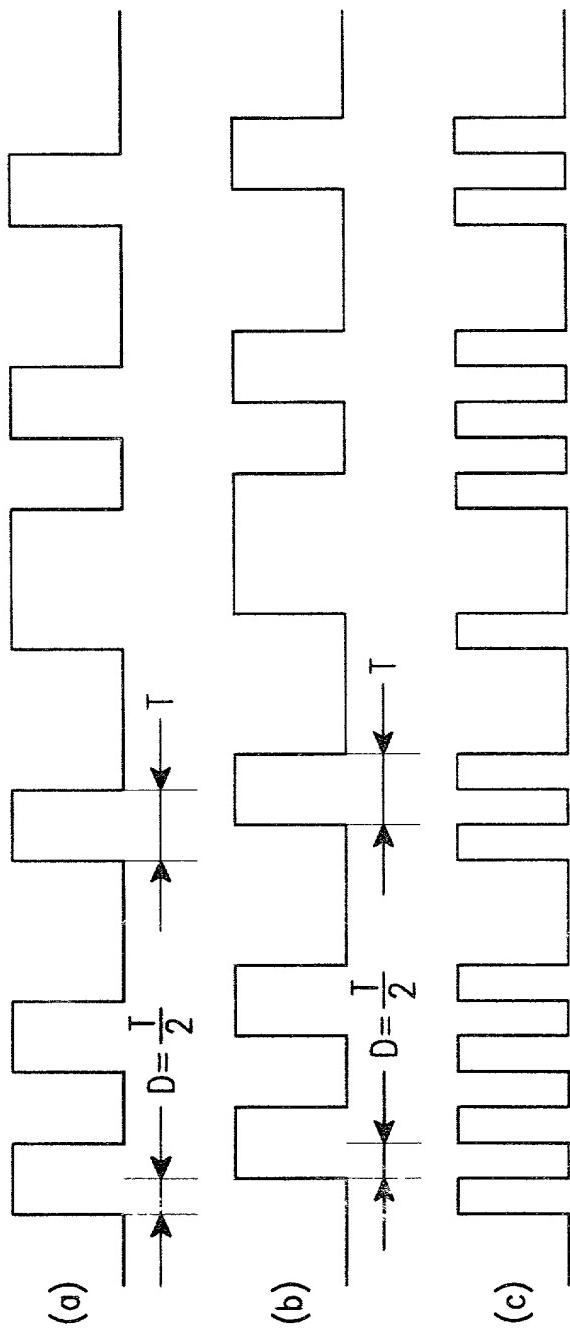


FIG. 4B

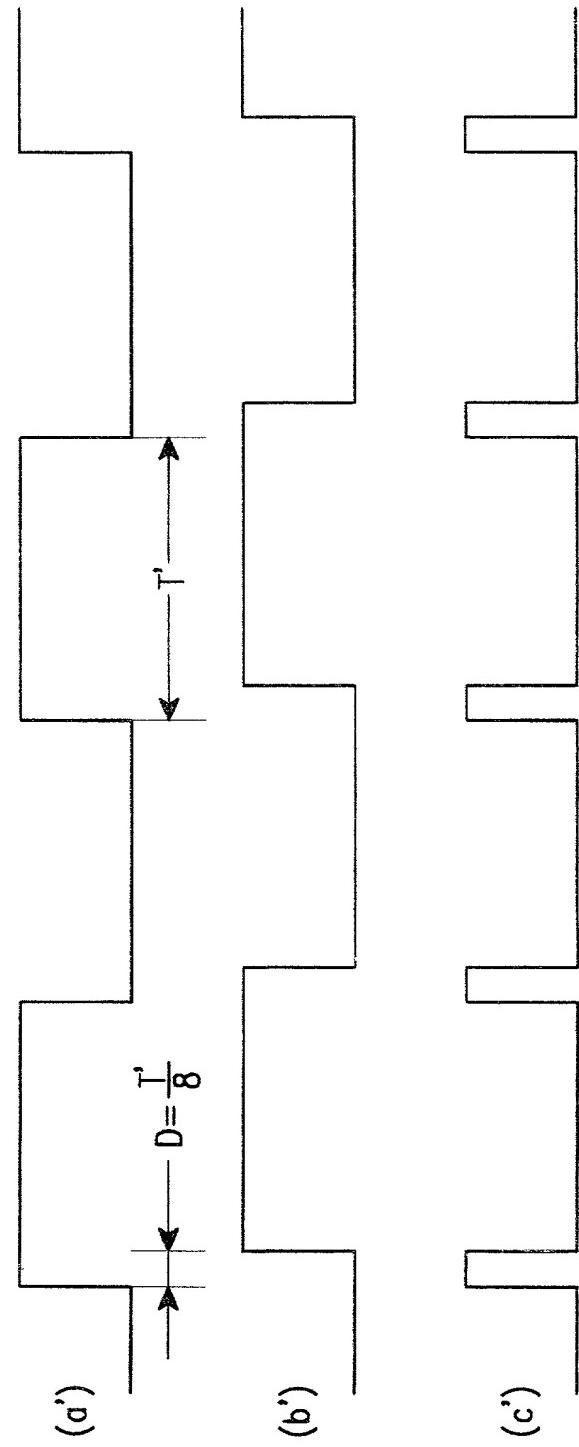
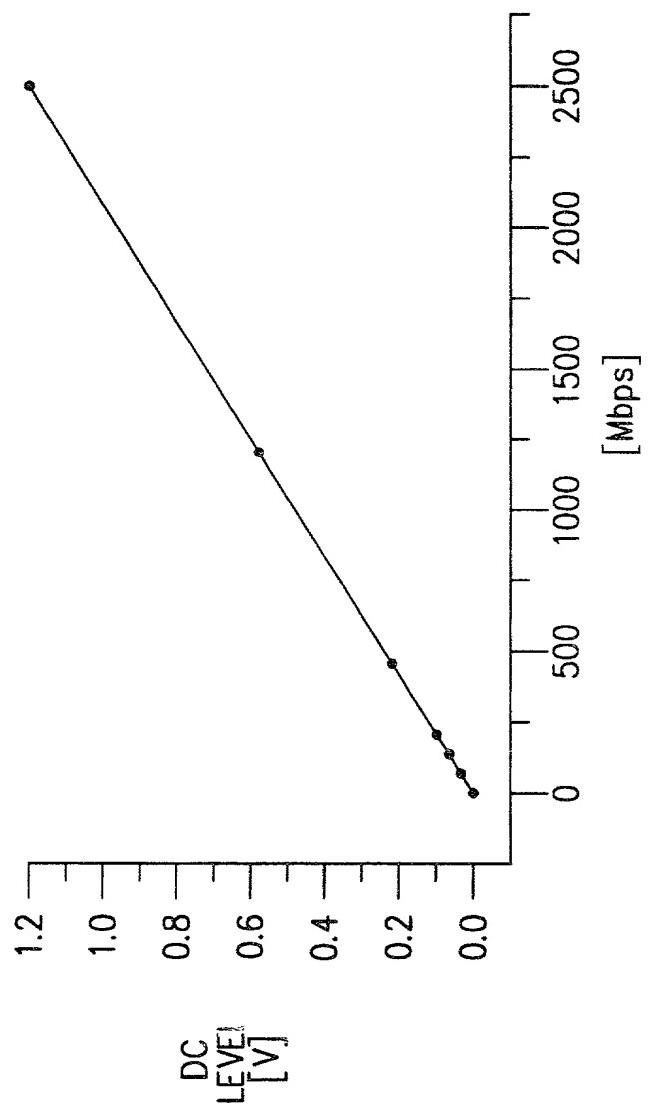


FIG. 5



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:

KWANG-JIN YANG et al.

Serial No.: *to be assigned*

Examiner: *to be assigned*

Filed: 20 July 2000

Art Unit: *to be assigned*

For: BIT-RATE INDEPENDENT OPTICAL RECEIVER AND METHOD THEREOF

**TRANSMITTAL OF DECLARATION**

Assistant Commissioner  
for Patents  
Washington, D.C. 20231

Sir:

This transmittal accompanies the original Declaration for the above-referenced application.

Respectfully submitted,

  
\_\_\_\_\_  
Robert E. Bushnell,  
Attorney for the Applicant  
Registration No.: 27,774

Suite 300, 1522 "K" Street, N.W.  
Washington, D.C. 20005  
(202) 408-9040

Folio: P56077  
Date: 7/20/00  
I.D.: REB/sb

## DECLARATION

AS A BELOW NAMED INVENTOR, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole (if only one name is listed below), or an original, first and joint inventor (if plural names are listed below), of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**TITLE: BIT-RATE INDEPENDENT OPTICAL RECEIVER AND METHOD THEREOF**

the specification of which either is attached hereto or otherwise accompanies this Declaration, or:

was filed in the U.S. Patent & Trademark Office on \_\_\_\_\_ and assigned Serial No. \_\_\_\_\_

and (if applicable) was amended on \_\_\_\_\_

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability and to the examination of this application in accordance with Title 37 of the Code of Federal Regulations §1.56. I hereby claim foreign priority benefits under Title 35, U.S. Code §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, or §119(e) of any United States provisional application(s), listed below and have also identified below any foreign applications for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

|                      |                   |                        |                                     |
|----------------------|-------------------|------------------------|-------------------------------------|
| 1999-32170           | Republic of KOREA | 05/08/1999             | Priority Claimed:<br>Yes [X] No [ ] |
| (Application Number) | (Country)         | (Day/Month/Year filed) |                                     |

|                      |           |                        |                |
|----------------------|-----------|------------------------|----------------|
| _____                | _____     | _____                  | Yes [ ] No [ ] |
| (Application Number) | (Country) | (Day/Month/Year filed) |                |

|                      |           |                        |                |
|----------------------|-----------|------------------------|----------------|
| _____                | _____     | _____                  | Yes [ ] No [ ] |
| (Application Number) | (Country) | (Day/Month/Year filed) |                |

I hereby claim the benefit under Title 35, U.S. Code, §120, of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of Title 35, U.S. Code, §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, The Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT International filing date of this application:

|                          |               |  |
|--------------------------|---------------|--|
| _____                    | _____         | (STATUS: patented, pending, abandoned) |
| (Application Serial No.) | (Filing Date) | (STATUS: patented, pending, abandoned) |

|                          |               |  |
|--------------------------|---------------|--|
| _____                    | _____         | (STATUS: patented, pending, abandoned) |
| (Application Serial No.) | (Filing Date) | (STATUS: patented, pending, abandoned) |

I hereby revoke all previously granted powers of attorney and appoint the following attorneys: Robert E. Bushnell, Reg. No. 27,774, Michael D. Parker, Reg. No. 34,973, and Henry M. Zykovic, Reg. No. 27,477 to prosecute this application and to transact all business in the U.S. Patent & Trademark Office connected therewith and with any divisional, continuation, continuation-in-part, reissue or re-examination application, with full power of appointment and with full power to substitute an associate attorney or agent, and to receive all patents which may issue thereon, and request that all correspondence be addressed to:

Robert E. Bushnell,  
Attorney-at-Law  
Suite 300, 1522 "K" Street, N.W.  
Washington, D.C. 20005-1202

Payor No. 008439  
Area Code: 202-638-5740

I HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §101 of Title 18 U.S. Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF FIRST OR SOLE INVENTOR: Kwang-Jin YANG Citizenship: Republic of KOREA

Inventor's signature: [Signature] Date: July 19, 2000  
Residence & Post Office Address: 244-1, Eonnam-ri, Kusong-myon, Yongin-shi, Kyonggi-do, Korea

FULL NAME OF SECOND JOINT INVENTOR: Jun-Ho KOH Citizenship: Republic of KOREA

Inventor's signature: [Signature] Date: July 19, 2000  
Residence & Post Office Address: 77, Kumi-dong, Puntang-gu, Songnam-shi, Kyonggi-do, Korea

FULL NAME OF THIRD JOINT INVENTOR: Gil-Yong PARK Citizenship: Republic of KOREA

Inventor's signature: [Signature] Date: July 19, 2000  
Residence & Post Office Address: SAN 14-1, Nongseo-ri, Kihung-up, Yongin-shi, Kyonggi-do, Korea

FULL NAME OF FOURTH JOINT INVENTOR: Bong-Sin KWARK Citizenship: Republic of KOREA

Inventor's signature: [Signature] Date: July 19, 2000  
Residence & Post Office Address: 51, Sunae-dong, Puntang-gu, Songnam-shi, Kyonggi-do, Korea

## DECLARATION

AS A BELOW NAMED INVENTOR, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole (if only one name is listed below), or an original, first and joint inventor (if plural names are listed below), of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**TITLE: BIT-RATE INDEPENDENT OPTICAL RECEIVER AND METHOD THEREOF**

the specification of which either is attached hereto or otherwise accompanies this Declaration, or:

was filed in the U.S. Patent & Trademark Office on \_\_\_\_\_ and assigned Serial No. \_\_\_\_\_.

and (if applicable) was amended on \_\_\_\_\_.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability and to the examination of this application in accordance with Title 37 of the Code of Federal Regulations §1.56. I hereby claim foreign priority benefits under Title 35, U.S. Code §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, or §119(e) of any United States provisional application(s), listed below and have also identified below any foreign applications for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

|                                    |                    |   |  |
|------------------------------------|--------------------|---|--|
| 32170/1999<br>(Application Number) | KOREA<br>(Country) | 5 August 1999<br>(Day/Month/Year filed) | Priority Claimed:<br>Yes [ <input checked="" type="checkbox"/> ] No [ <input type="checkbox"/> ] |
|------------------------------------|--------------------|---|--|

|                      |           |                        |  |
|----------------------|-----------|------------------------|--|
| (Application Number) | (Country) | (Day/Month/Year filed) | Yes [ <input type="checkbox"/> ] No [ <input type="checkbox"/> ] |
|----------------------|-----------|------------------------|--|

|                      |           |                        |  |
|----------------------|-----------|------------------------|--|
| (Application Number) | (Country) | (Day/Month/Year filed) | Yes [ <input type="checkbox"/> ] No [ <input type="checkbox"/> ] |
|----------------------|-----------|------------------------|--|

I hereby claim the benefit under Title 35, U.S. Code, §120, of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application(s) in the manner provided by the first paragraph of Title 35, U.S. Code, §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, The Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

|                          |               |  |
|--------------------------|---------------|--|
| (Application Serial No.) | (Filing Date) | (STATUS: patented, pending, abandoned) |
|--------------------------|---------------|--|

|                          |               |  |
|--------------------------|---------------|--|
| (Application Serial No.) | (Filing Date) | (STATUS: patented, pending, abandoned) |
|--------------------------|---------------|--|

I hereby revoke all previously granted powers of attorney and appoint the following attorneys: Robert E. Bushnell, Reg. No. 27,774, Michael D. Parker, Reg. No. 34,973, and Darren R. Crew, Reg. No. 37,806, to prosecute this application and to transact all business in the U.S. Patent & Trademark Office connected therewith and with any divisional, continuation, continuation-in-part, reissue or re-examination application, with full power of appointment and with full power to substitute an associate attorney or agent, and to receive all patents which may issue thereon, and request that all correspondence be addressed to:

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I HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 U.S. Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Additional inventors are being named on separately numbered sheets attached hereto.